https://dx.doi.org/10.22161/ijaers.4.7.3 *ISSN: 2349-6495(P) | 2456-1908(O)*

Design and Analysis of 8x8 Wallace Tree Multiplier using GDI and CMOS Technology

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Abstract— *Multiplier is a small unit of an arithmetic circuit that is widely used in Digital filters, Digital Signal Processing, microprocessors and communication applications etc. In today's scenario compact and small digital devices are critical concern in the field of VLSI design, which should perform fast as well as low power consumption. Optimizing the delay, area and power of a multiplier is a major design issues, as area and speed are usually conflicting constraints. A Wallace tree multiplier is an improved version of tree base multiplier.*

The main aim of this paper is a reconfigurable 8x8 Wallace Tree multiplier using CMOS and GDI technology. This is efficient in power and regularity without increase in delay and area. The generation of partial products in parallel using AND gates. The addition of partial products is reducing using Wallace Tree which is divided into levels. Therefore there will be a certain reduction in the power consumption, since power is provided only to the level that is involved in computation and the remaining two levels remain off.

Keywords— Multiplier, GDI ,CMOS, Wallace tree .

I. INTRODUCTION

Arithmetic operations are penetrating into more and more applications with the advances in VLSI technology. The root operation found in most arithmetic components are binary addition and multiplication and division, which improves the performance using low-power, area efficient circuits operating at higher speed[1].

Multiplication is an operation that uses frequently in DSP and much other application. It occupies more area that it consumes large delay when compared to adder. Therefore it is imperative that special techniques be used to speed up the calculation of the product while maintaining a reasonable area. Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. In addition, each resulting bits are depending on its corresponding In case of addition each of resulting output bits are depending on its inputs. It is important operation because it involves a carry ripple step i.e. the carry from the previous bits addition should propagates to next bit of addition.

II. PROCESS OF MULTIPLICATION

In digital electronics the multiplication operation is very simple and easy to access**.** The multiplier uses addition and shift left operations for calculating the product of two binary numbers. Techniques involve in computing a set of the partial products, thereafter summation of partial products together.

2.1 Multiplication involves two steps:

2.1.1 Partial Product Generation

2.1.2 Their Summation

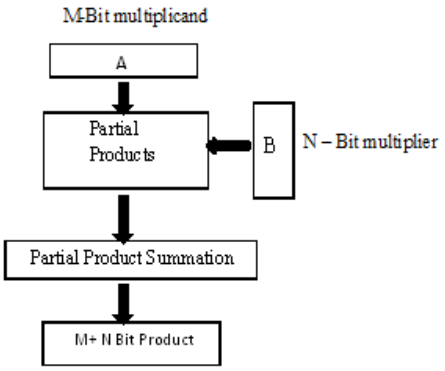

Fig 2.1: *Multiplier Block Diagram*

The figure 2.1 shows the multiplication process of two unsigned binary digits. In the multiplication process the first digit is called Multiplicand and the second digit is called multiplier and the first step in the multiplication is called partial product. In the partial product row if the multiplier bit is "1" then partial product row is same as multiplicand digit, if the multiplier bit is "0" then the partial product row is zero.

An example of multiplication that is consisting product of the two unsigned (positive) binary numbers radix 2 given below,

1011 (this binary number represents 11)
X 1010 (this binary number represents 10)
0000 (1011 x 0)
1010 (1010 x 1, shifted one position to left)
0000 (1010 x 0, shifted two position to left)
+1010 (1010 x 1, shifted three position to left)
01101110 (This binary number represents 110)

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III. WALLACE MULTIPLIER

Scientist Chris Wallace in 1964 introduced an easy and simple way of summing the partial product bits in the parallel using the tree of the Carry Save Adders which is known as "Wallace Tree"[2]. A typical Wallace tree architecture is shown in figure 3.1.

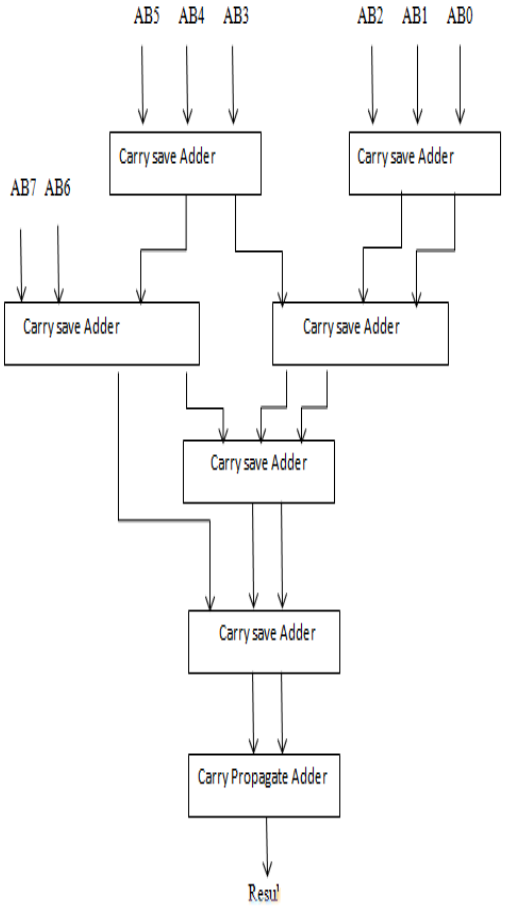

Fig.3.1: Wallace Multiplier

Wallace multiplier includes steps to multiply two numbers .The first step is formation of the bit products. Then carry save adder reduces bit product matrix into two row matrix. After that the remaining two rows are summed by using the fast carry propagate adder to produce the final result. However the process become complex, the multiplier with delay proportional to logarithm of operand size n [3]. This algorithm reduced the partial product at a rate of log3/2 N/2. By using carry-save adder the need of carry propagation in the adder is avoided and latency of one addition is equal to gate delay of adder.

IV. CIRCUIT DESIGN

4.1 OR Gate:

Schematic diagram of GDI based OR gate is shown in figure 4.1. The OR gate is one of the basic digital logic gate. Basically, the function of the OR effectively finds the maximum digit between two binary digits. In OR gate one out of three inputs is fixed, connected to Vdd,While other two inputs are variable can be logic High (logic 1)or logic Low(logic 0). The output of the OR Gate gives logic high when one or both of the input to the gate are logic High, if both input to the gate are logic low then the result will be logic low.

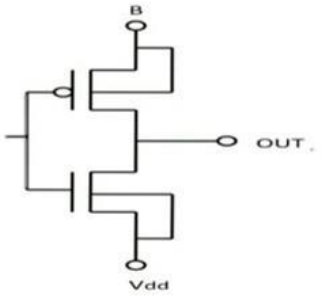

Fig.4.1: GDI based OR gate

4.2 AND Gate:

Schematic diagram of GDI based AND gate is shown in figure 4.2. The AND gate is used for the product of two binary digits. Basically, the function of the AND effectively finds the minimum digit between two binary digits. It gives high output (logic 1) only if both inputs to AND gate are logic high (logic 1). And if none or only one input to AND gate is high, than a low output is generated. Therefore, the output is always low ('0') except when all inputs are high ('1's)

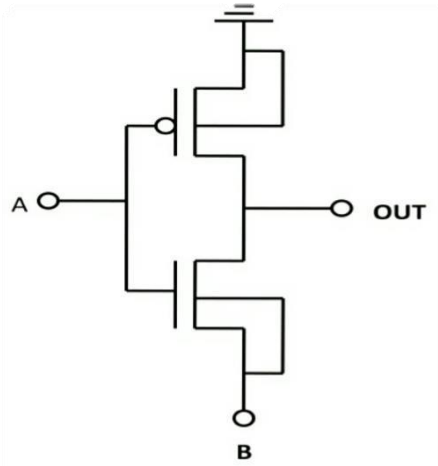

Fig.4.2: GDI based AND gate

4.3 XOR Gate:

Schematic diagram of GDI based XOR gate is shown in figure 4.3. When inputs are different then output is logic high and both inputs are same either logic high or logic low then output will become logic low (logic 0).

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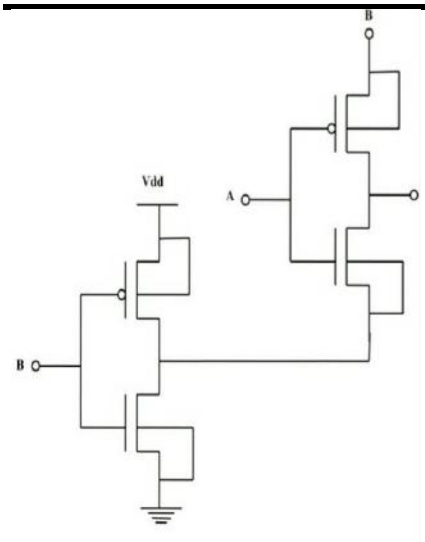

Fig.4.3: GDI based XOR gate

4.4. Half Adder:

Half adder has two inputs, generally denoted A and B, and two outputs, the sum (S) and carry (C). Essentially the output of a half adder is the sum of two one-bit numbers , XOR operation of the two inputs A and B produces output Sum, AND operation of the input produces Carry as a output. Although by itself, a half adder is not such useful, it can be used as a building block for larger adding circuits (Full Adder) [4]. In fig a logic & block diagram of half adder (HA) is shown in figure 4.4.

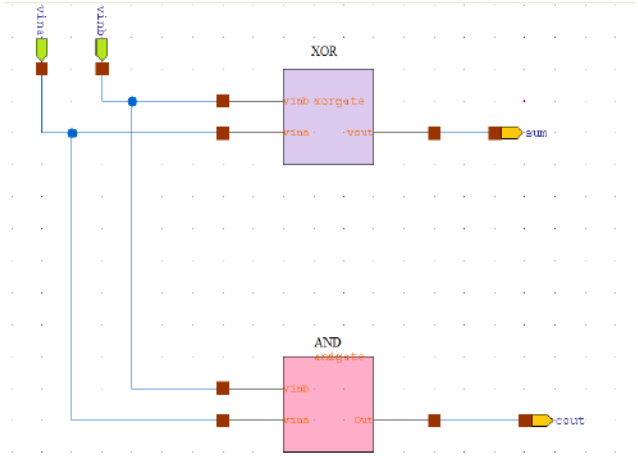

Fig.4.4:GDI based Half Adder

4.5 Full Adder:

Full Adder is used to add three inputs Vina, Vinb and Vinc to produce sum and carry out (Cout). Vinc input is the carry generated from previous stage[4]. Schematic diagram of GDI based full adder circuit is shown in figure4.5.

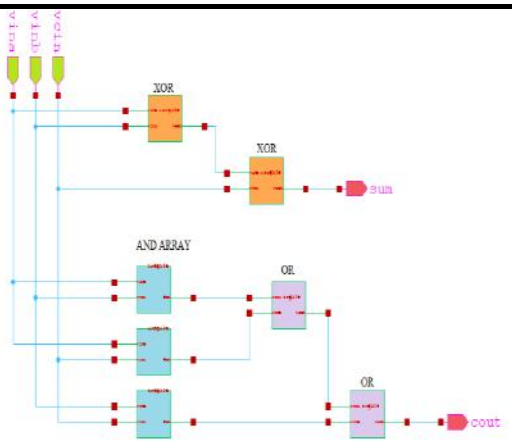

Fig.4.5: GDI based Full Adder

4.6 Compressor:

For three inputs full adder can be used to summation, but for more than three input another types of adder are used which is called compressor circuit. Compressor circuit is used to add four or five input. Compressor circuit is used for addition of more than three inputs. The 4:2 Compressor has 5 inputs to generate 3 outputs Sum, Carry and Cout. The input Vcin is the output from a previous lower significant compressor and the Cout output is for the compressor in the next significant stage [3]. Circuit diagram of 4:2 compressor is shown in figure 4.6 and Circuit diagram of 5:2 compressor is also shown in figure 4.7.

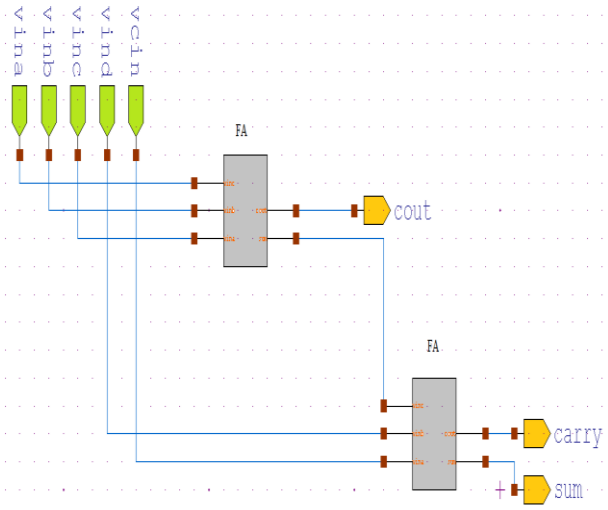

Fig.4.6: GDI based 4:2 Compressor

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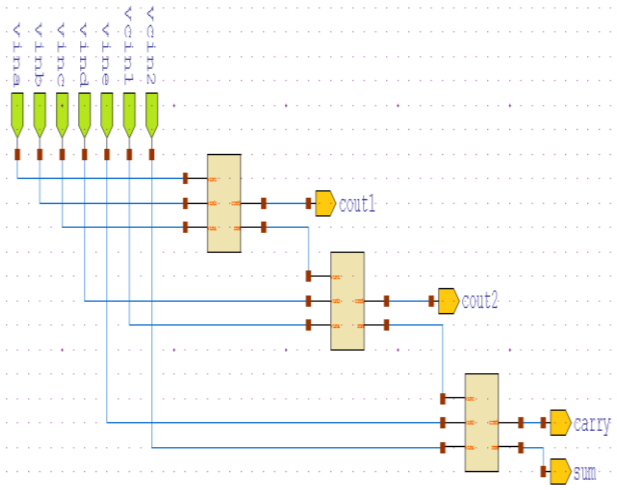

Fig.4.7: GDI based 5:2 Compressor

4.8 8-Bit Multiplier:

8x8 bit multiplier based on Wallace Tree is efficient in terms of the power and the regularity without increase in the delay as well as in the area. The idea involves generation of partial products in the parallel using the AND gates. Furthermore, the addition of the partial products is done using the Wallace tree, which is hierarchal, divided into levels. There will be a reduction in power consumption, since the power is provided only to level that is involved in the computation [5].

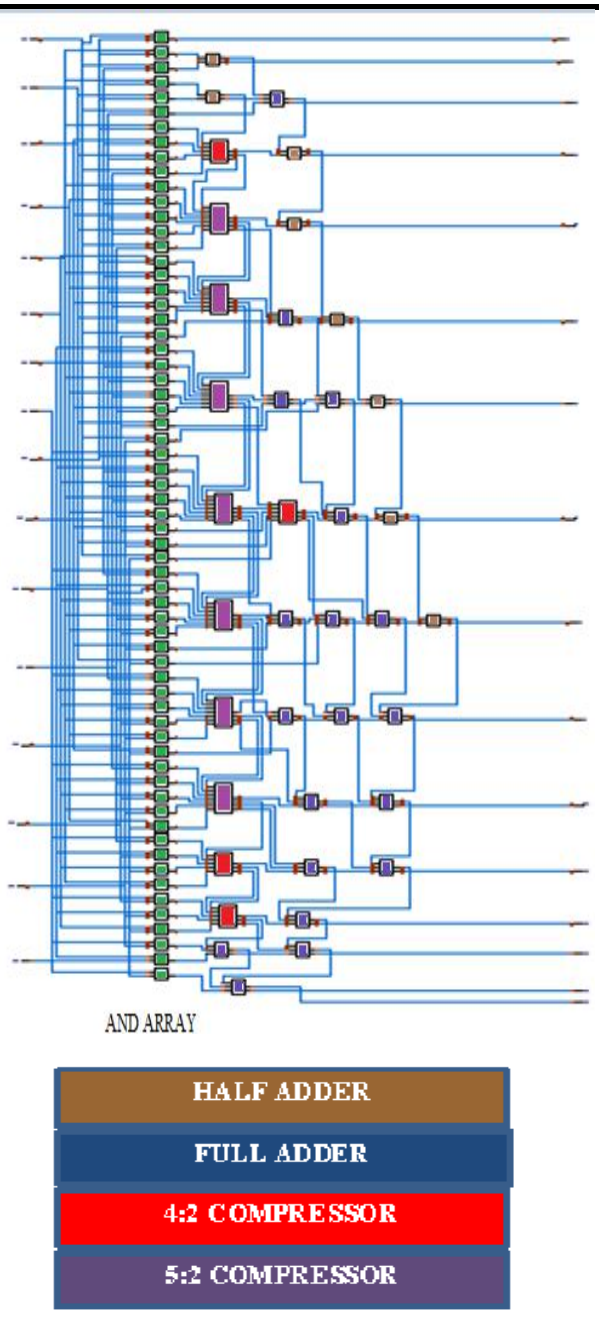

Fig.4.8: GDI based 8-Bit Multiplier Schematic

V. RESULT AND ANALYSIS

This paper shows comparison of power calculation, Delay calculation and area in terms of transistor and the design has been implemented and simulated using Tanner Tool in 180nm technology with operating voltage of approximately 1.8V. Comparison of delay at different power supply voltage of different bit multiplier is shown in figure 5.1.

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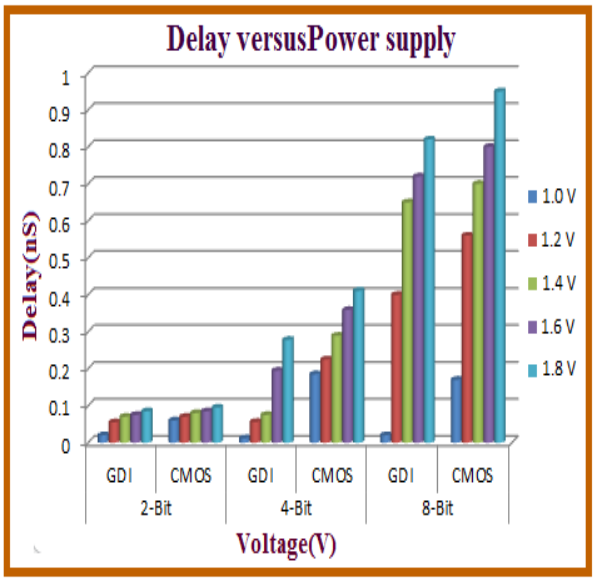

Fig.5.1: Comparison of Delay at different supply

VI. CONCLUSION

Multiplier is one of the important units for most of digital circuits. Low power dissipation, minimum propagation delay and area minimization of the circuit are major concern. Wallace tree multiplier based on GDI technology occupies smaller silicon area than the conventional Wallace tree multiplier. At different power supply, propagation delay are calculated and shown in the graph 5.1. The comparison at 1.8V power supply shows the delay of Wallace tree 8-Bit multiplier GDI based and CMOS based are 0.02nS and 0.17nS respectively. Thus GDI based circuit helps us to reduce propagation delay, power dissipation compare to CMOS based circuits.

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